Electronic Version
Stylesheet Version v1.1.1

# Description

# MICROCONTROLER WITH EXPANDABLE PROGRAM MEMORY BANKS

## BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a method for managing a program memory and more particularly, to a method for managing an external program memory of a microprocessor.

[0003] 2. Description of the Prior Art

[0004] Intel Corporation generally refers to a microprocessor as an MCS (Micro Computer System) and the MCS-51/52 series microprocessor developed by the Intel Corporation is commonly used in industry. Generally speaking, a microprocessor comprises a small memory and a few I/O ports. Take the MCS-51 microprocessor for example; it comprises a program memory of 4K bytes, a data memory of 128 bytes, and 32 I/O ports. The MCS-52 series micro-

processor comprises a program memory of 8K bytes and a data memory of 256 bytes. The MCS-51/52 series of microprocessors features an 8-bit CPU. The program memory is a read-only memory (ROM) for storing a program written by a user. The data memory is a random-access memory for storing data temporarily while the CPU executes a program. The capacity of the memory of the MCS-51/52 series microprocessor can be externally expanded to 64K bytes.

[0005] An external program memory with capacity of 64K bytes is still not large enough if the user needs to write lengthy code or use a large array table. To solve this problem, the capacity of the external program memory of the microprocessor can be substantially expanded by switching a plurality of memory banks when the user uses the extra pins of the microprocessor as decode lines to set an address for an external program memory with capacity of over 64K bytes. If the external program memory is one memory device with large capacity, the extra pins of the microprocessor can be address lines. If there are several external program memory devices with smaller capacity, the extra pins of the microprocessor can be used to select the memory chips. Because the largest capacity of the ex-

ternal program memory of the microprocessor is 64K bytes, 64k bytes can be taken as a unit (a page) when the microprocessor switches the memory banks. Further, an interrupt vector table is usually stored at a specific address of the external program memory, and the microprocessor searches for the interrupt vector table at the specific address in a current page immediately when an interrupt occurs. Because the microprocessor cannot switch the plurality of memory banks when the interrupt occurs, an error occurs when the microprocessor cannot find the interrupt vector table in the current page. To solve this problem, a common area in each memory bank is reserved for storing the interrupt vector table, interrupt service routines, common program library, and a memory bank switching routine, etc.. This ensures that the microprocessor can find the interrupt vector table in the current page (can be any page) and, when the interrupt is served, continue executing the interrupted program.

[0006] Fig. 1 is a diagram of an external program memory 12 according to the prior art. The capacity of the external program memory 12 of the MCS-51/52 series microprocessor is expanded to 512K bytes by switching the plurality of memory banks. The external program memory 12 is di-

vided into 8 pages. The capacity of each page is 64K bytes but a common area in each page with certain capacity (ex. 10K bytes)is reserved for storing the interrupt vector table, the interrupt service routines, the common program library, and the memory bank switching routine, etc.. For example, when the microprocessor has to execute a program B in page 2 while executing a program A in page 1, it will call the bank switching routine in the common area. The memory bank switching routine stored in the common area will set the page number to 2, then the microprocessor can access the program B in page 2. After executing the program in the page 2, the microprocessor will return to the program A by calling the bank switching routine in the common area, and the memory bank switching routine will switch the page number from 2 to 1, so the microprocessor can return to the address of the program A in page 1 to continue executing the program A. Further, when the interrupt occurs, the microprocessor accesses the interrupt vector table stored in the common area to access and execute the interrupt service routines according to the content of the interrupt vector table. The microprocessor then comes back to the original address of the program to continue executing the interrupted pro-

gram. The interrupt service routines and the interrupt vector table are stored in the common area of each page, thus, when accessing the interrupt service routines and the interrupt vector table, it is not necessary to switch the pages.

[0007] According to the foregoing description, though the largest capacity of the external program memory of the MCS-51/52 series microprocessor is 64K bytes, the external program memory can be further expanded by switching the plurality of memory banks when using the extra pins of the microprocessor as the decode lines to set the address of the external program memory with capacity of over 64K bytes. However, each memory bank has to reserve a certain space for the common area to store the interrupt vector table, the interrupt service routines, the common program library, and the memory bank switching routine, etc.. These multiple common areas mean the space of the external program memory is not used efficiently.

## SUMMARY OF INVENTION

[0008] It is therefore a primary objective of the claimed invention to provide a method for managing an external program memory of a microprocessor to solve the above-

mentioned problem.

[0009] According to the claimed invention, a microcontroller with expandable memory banks comprises a microprocessor, a plurality of memory banks, which have a storage space that is larger than the addressing capability space of the microcontroller, connected to the microprocessor for storing data, programs and interrupt service routines in one of the memory banks, a memory bank control circuit, and a multiplexer for connecting the microprocessor with the plurality of memory banks. The multiplexer comprises a first input connected to an output of the microprocessor for bank switching during normal operation, a second input connected to a predetermined value corresponding to the memory bank storing the interrupt service routines, and a selecting port for receiving a selection signal generated by the memory bank control circuit. The memory bank control circuit generates the selection signal according to an interrupt signal and a microprocessor interrupt service routine execution end signal. The multiplexer switches to output a page selection signal from the output of the microprocessor or a predetermined page selection signal according to the selection signal so that the microprocessor can access the interrupt service routines when

the interrupt occurs.

[0010] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

## Brief Description of Drawings

[0011] Fig. 1 is a diagram of an external program memory allocation according to a prior art.

[0012] Fig. 2 is a diagram of an external program memory allocation of a microprocessor according to a present invention.

[0013] Fig. 3 is a diagram of the microprocessor connected to the external program memory ofFig.2.

## Detailed Description

[0014] Fig. 2 is a diagram of the arrangement of a plurality of memory pages in an external program memory 22 according to the present invention. In the prior art previously described, the multiple common areas mean the space of the external program memory 22is not used efficiently. To decrease the space occupied by the common area, the present invention omits the interrupt service

routines from each common area 24 in each memory page and only stores interrupt service routines 26 in one of the memory pages in the external program memory 22. When an interrupt occurs, the microprocessor switches to the memory page storing the interrupt service routines 26 to access the interrupt service routines 26.

[0015] Because the space occupied by the common area in each memory page is reduced, the storage space of each memory page becomes larger, and the memory pages will be switched less frequently. For instance, the capacity of the external program memory 22 is 512K bytes. The external program memory 22 is divided into 8 pages. The capacity of each page is 64K bytes but a common area in each page with capacity of 10K bytes is reserved. Assume the total size for the interrupt service routines is 4K bytes. Then if only page 0 of the memory bank stores the interrupt service routines 26, the capacity of each memory page (except page 0 of the memory bank) is increased from 54K bytes to 58K bytes and the total increased capacity is 28K (4K*(8-1)=28K). When the interrupt occurs, a CPU of the microprocessor pushes the current program counter address and a page number of the current memory page onto a stack, and then switches the current

memory page to page 0 of the external program memory 22 to execute the interrupt service routines. The present invention uses the memory bank control circuit and the multiplexer to switch the microprocessor to page 0 of the memory bank to execute the interrupt service routines when the microprocessor is interrupted. The multiplexer and a microprocessor interrupt service routine execution end signal are used to omit the interrupt service routines from each common area 24 in each memory page and only stores the interrupt service routines 26 in one of the memory pages in the external program memory 22.

[0016] Fig. 3 is a diagram of a microprocessor 20 connected to the external program memory 22 according to the present invention. A port P0 and a port P2 directly connected to the external program memory 22 are used to set addresses and access the memory banks of the external program memory 22. A port P1 of the microprocessor is connected to the external memory 22 via a multiplexer 24, which comprises an input A, an input B, an output C, and a selecting input D. The input A of the multiplexer 24 connected to the port P1 of the microprocessor 20 is used to input a page number of the external program memory 22 by the microprocessor 20. The input B of the multi-

plexer 24 is connected to a predetermined page number signal ("Set" shown in Fig. 3), wherein the predetermined page number signal is the page number of the memory page storing the interrupt service routines. The output C of the multiplexer 24 is connected to the external program memory 22, and is used to select the page of the external program memory 22. The selecting input D of the multiplexer 24 is connected to an output ("Sel" shown in Fig.3) of a memory bank control circuit 23. The memory bank control circuit 23 outputs a logic low signal if the microprocessor is not executing interrupt service routines. The multiplexer 24 outputs a page number signal from the input A according to the logic low signal so that the microprocessor 20 can switch and access the memory pages of the external program memory 22 normally. When the microprocessor 20 receives an interrupt request while executing a program, the memory bank control circuit 23 will raise the output signal to a logic high. Hence, the multiplexer 24 outputs the predetermined page number signal from the input B so that the microprocessor 20 will be switched to the memory page storing the interrupt service routines and execute the interrupt service routines. Because when an interrupt occurs the microprocessor 20

cannot switch the memory page and can only execute a program in the memory page storing the interrupt service routines, a user has to store a program, which is called while the microprocessor 20 executes the interrupt service routines, and the interrupt service routines in the same memory bank.

[0017] According to the foregoing description, the present invention omits the interrupt service routines from the common area in each memory page and only stores interrupt service routines in one of the memory pages in the external program memory 22. When the microprocessor 20 switches the memory banks of the external memory 22, the multiplexer 24 connects the port P1 (a page selector) of the microprocessor 20 to the external program memory 22. Further, the memory bank control circuit 23 selects a page number signal outputted to the external program memory 22 from the multiplexer 24 according to the interrupt signal and the microprocessor interrupt service routine execution end signal. When the memory bank control circuit 23 outputs the logic low signal, the multiplexer 24 outputs the page number signal driven by the microprocessor. When the memory bank control circuit 23 outputs the logic high signal, the multiplexer 24 outputs

the predetermined page number signal so that the microprocessor 20 can switch to the memory bank storing the interrupt service routines and execute the interrupt service routines.

[0018] In contrast to the prior art, the microprocessor 20 can use the multiplexer to switch the memory page when the interrupt occurs so that the interrupt service routines can be omitted from each common area 24 in each memory page. Because the space occupied by the common area in each memory page is reduced, the effective storage space of each memory page is larger, and the memory pages will be switched less frequently. The prior art has to reserve a certain quantity of space in each memory bank for the common area comprising the interrupt service routines when expanding the capacity of the external program memory using switched memory pages. These multiple common areas mean the space of the external program memory is not used efficiently. Compared with the prior art, the present invention uses the storage space of the external memory more efficiently.

[0019] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accord-

ingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.